Please amend the claims as follows:

1. (Currently Amended) A method of operating a memory management system to resolve contention for access to a data bus extending to a plurality of memories; said method comprising the steps of:

generating requests for a ~~the~~ reading and writing of data in ~~by~~ said memories;

generating signals indicating a ~~the~~ busy / idle state of each of said memories;

extending said signals from said memories to ~~said~~ an access flow regulator over a request bus comprising separate conductors independent of said data bus with each conductor being individual to a different one of said memories;

operating said access flow regulator in response to a ~~said~~ receipt of said signals to determine a ~~the present~~ busy / idle state of each of said memories;

applying said requests to said access flow regulator; and

operating said access flow regulator in response to a determination that one of said memories is currently idle for granting a request ~~to~~ for access to said data bus for a ~~the~~ reading or writing of a data in ~~by~~ said one memory.

2. (Currently Amended) The method of claim 1 including the further steps of:

operating said access flow regulator in response to a determination that none of said memories is currently idle for buffering said request ~~to define a buffered request~~ until one of said memories becomes idle; and

serving said buffered request when said one of said memories becomes idle.

3. (Currently Amended) The method of claim 1 including the further steps of:

determining that a plurality of requests are concurrently seeking access to an idle one of said memories;

granting one of said requests access to said idle memory; and

buffering others ~~the other~~ of said requests until one of said memories becomes idle and available to serve said other request.

4. (Currently Amended) The method of claim 1 wherein the step of generating signals includes the steps of:

monitoring a ~~the~~ present busy / idle state of each of said memories;

generating a busy signal for a memory only when ~~for the time duration~~ the memory is in a busy state;

generating an idle signal for a memory immediately upon a determination that the memory has assumed an ~~and~~ idle state;

extending said idle signal over said request bus to said access flow regulator; and

operating said access flow regulator to grant a waiting request access to said memory immediately upon the receipt of said idle signal by said access flow regulator.

5. (Currently Amended) The method of claim 1 wherein said system further comprises a plurality of state controllers each of which is individual to a different one of said memories, ~~said system further comprises a~~ said request bus connects ~~connecting~~ said access flow regulator with said memories via said state controllers; said method ~~step of transmitting a read request~~ includes the steps of:

operating said access flow regulator to select an idle one of said memories that is to receive a request;

transmitting said request from said access flow regulator over said request bus to the state controller individual to said idle one of said memories;

extending said request from said state controller to said idle memory individual to said state controller; and

operating said state controller to control the operation of the memory unique to said state controller.

6. (Currently Amended) The method of claim 5 wherein said step of operating said state controller includes the steps of:

determining a ~~the~~ present occupancy level of ~~said~~ a selected memory;

transmitting said request to said selected memory if said present occupancy level is not exceeded; and

buffering said request in said access flow regulator if said occupancy level of said selected memory is exceeded.

7. (Currently Amended) The method of claim 1 including the further steps of:

embodying said system into a network node having incoming and outgoing links;

applying requests received by said links to said access flow regulator; and

processing said requests for granting access to said memories via said data bus to control the data throughput of said network node.

8. (Currently Amended) The method of claim 1 including the further steps of:

operating said system to concurrently process a plurality of requests for access via said data bus to idle ones of said memories; and

buffering said requests that are received when an idle one of said memories is not available.

9. (Currently Amended) The method of claim 5 wherein said step of extending said signals to said access flow regulator includes the steps of:

extending said signals from said memories over separate conductors of said request bus via said state controllers to said access flow regulator with each of said conductors being individual to a different one of said memories; and

operating said access flow regulator to detect the signal on each conductor to determine a ~~the~~ busy / idle state of the memory unique to each said conductor.

10. (Currently Amended) The method of claim 9 including the further steps of:

extending said signals ~~signal~~ over said separate conductors of said request bus from said state controllers to said access flow regulator, each conductor of said request bus extends between said access flow regulator and a different one of said state controllers.

11. (Currently Amended) A memory management system adapted to resolve ~~for resolving~~ contention for access to a data bus extending to a plurality of memories; said system comprising:

apparatus for generating requests for access to said data bus for a ~~the~~ reading and writing of data in ~~by~~ said memories;

apparatus for generating signals indicating a present ~~the~~ busy / idle state of each of said memories;

apparatus independent of said data bus for extending said signals from said memories to an ~~said~~ access flow regulator over a request bus comprising separate conductors with each conductor being individual to a different one of said memories;

apparatus for operating said access flow regulator in response to a ~~said~~ receipt of said signals to determine a ~~the~~ present busy / idle state of each of said memories;

apparatus for applying said requests to said ~~an~~ access flow regulator; and

apparatus for operating said access flow regulator in response to a determination that one of said memories is currently idle for granting a request for access to said data bus for the reading or writing of ~~a~~ data in ~~by~~ said one memory.

12. (Currently Amended) The system of claim 11 further including:

apparatus for operating said access flow regulator in response to a determination that none of said memories is currently idle for buffering a ~~said~~ request ~~to define a buffered request~~ until one of said memories becomes idle; and

apparatus for granting said buffered request when said one of said memories becomes idle.

13. (Currently Amended) The system of claim 11 further including:

apparatus for determining that a plurality of requests are concurrently seeking access to an idle one of said memories;

apparatus for granting one of said requests access to said one idle memory; and

buffering ~~the other~~ others of said requests until one of said memories becomes available to serve said other request.

14. (Currently Amended) The system of claim 11 further including:

apparatus for monitoring a ~~the~~ present busy / idle state of each of said memories;

apparatus for generating a busy signal only when ~~for~~ the ~~time duration a~~ memory is in a busy state;

apparatus for generating an idle signal immediately upon a determination that a memory has assumed and idle state;

apparatus for extending said idle signal over said request bus to said access flow regulator; and

apparatus for operating said access flow regulator to grant a waiting request access via said data bus to said memory immediately upon the receipt of said idle signal by said access flow regulator.

15. (Currently Amended) The system of claim 11 further comprising:

a plurality of state controllers each of which is individual to a different one of said memories;

said ~~a~~ request bus ~~connecting~~ connects said access flow regulator with said memories via said state controllers;

apparatus for operating said access flow regulator to select an idle one of said memories that is to receive a request;

apparatus for transmitting said received request from said access flow regulator over said request bus to the state controller individual to said idle one of said memories; and

apparatus for extending said received request from said state controller to said idle ones of said memories.

16. (Currently Amended) The system of claim 15 wherein said apparatus for operating said state controller includes:

apparatus for determining a ~~the~~ present occupancy level of ~~said~~ a selected memory;

apparatus for transmitting said received request to said selected memory if said present occupancy level is not exceeded; and

apparatus for buffering said received request in said access flow regulator if said occupancy level of said selected memory is exceeded.

17. (Currently Amended) The system of claim 15 further including:

apparatus for embodying said system into a network node having incoming and outgoing links;

apparatus for applying requests received by said links to said access flow regulator; and

apparatus for processing said request for granting access via said data bus to said memories to control the data throughput of said network node.

18. (Currently Amended) The system of claim 11 further including:

apparatus for operating said system to concurrently process a plurality of requests for access via said data bus to idle ones of said memories; and

apparatus for buffering said requests that are received when an idle one of said memories is not available.

19. (Currently Amended) The method of claim 13 wherein said apparatus for extending said signals comprises:

apparatus for extending said signals from said memories over separate conductors of said request bus via said state controllers to said access flow regulator with each of said conductors being ~~is~~ individual to a different one of said memories; and

apparatus for operating said access flow regulator to detect the signal on each said conductor of said request bus to determine ~~the~~ a busy / idle state of the memory unique to each said conductor.

20. (Currently Amended) The method of claim 19 further includes:

said apparatus for extending said received signals ~~signal~~ over said separate conductors of said request bus from said state controller to said access flow regulator

~~from said state controllers~~, wherein each said conductor extends between said access flow regulator and a unique one ~~on~~ of said state controllers.